UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,967	11/27/2001	Takashi Yamada	P 28403201F171	8085

7590 07/10/2003

Pillsbury Winthrop LLP
Intellectual Property Group
P O BOX 10500
McLean, VA 22102

EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,967	YAMADA ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *9-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,21 and 24-26* is/are rejected.

7)☒ Claim(s) *4,5,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the amendment filed April 28, 2003.

Priority

2. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application filed in Japan on 6/12/00. A claim for priority under 35 U.S.C. 119(a)-(d) cannot be based on said application, since the United States application was filed more than twelve months thereafter. The oath that was filed has 6/12/00 as the filing date. Additionally, the priority document has 6/12/00 on its cover.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as obvious over Lee (U.S. Patent No. 5,959,322) in view of Malik et al. (U.S. Patent No. 6,294,423).

In regards to claim 1, Lee discloses the following:

a) an element substrate (10) including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate (26) with a dielectric film (20) interposed there between (For example: See Figure 2);

b) element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film (For Example: See Figures 2, 8 and 14);

c) an impurity diffusion source buried in said groove to be contacted with said bottom surface of said semiconductor layer (For Example: See Figure 2 and 14); and

d) a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode (For Example; See Figure 2 and 14).

In regards to claim 1, Lee fails to disclose the following:

a) groove being formed to have an increased width portion in said dielectric film, said dielectric film of said increased width portion being receded laterally as to expose a bottom surface of said semiconductor layer and such that the width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer.

However, Malik et al. ("Malik") discloses a groove formed with an increased width portion that exposes the bottom and the width of the groove in the dielectric film is greater than that of the groove in the semiconductor layer (For Example: See Figure 5, Figure 10 and Column 1 Lines 34-48). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a groove with an increased width portion and the width of the groove in the dielectric film is greater than that

of the groove in the semiconductor layer as disclosed in Malik because it aids in isolating various integrated semiconductor devices.

Additionally, since Lee and Malik are both from the same field of endeavor, the purpose disclosed by Malik would have been recognized in the pertinent art of Lee.

In regards to claim 2, Lee discloses the following:

a) groove is formed deep enough to reach the inside of said semiconductor substrate after penetration through said dielectric film (For Example: See Figures 2, 7, 8 and 14);

b) a trench capacitor (16) (For Example: See Figure 2); and

c) storage electrode (18) (For Example: See Figure 2).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as obvious over Lee (U.S. Patent No. 5,959,322) in view of Malik et al. (U.S. Patent No. 6,294,423) and Applicant's Prior Art Drawing.

In regards to claim 3, Lee fails to disclose the following:

a) a buried strap for use as said impurity diffusion source is formed and buried in said groove portion overlying said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof, and wherein this buried strap is covered with a cap insulation film with the gate electrode of said transistor embedded to overlie said cap insulation film.

However, Applicant's Prior Art Drawing discloses a strap (3) buried in a groove (For Example: See Figure 37). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a strap as disclosed in Applicant's Prior Art Drawing because it aids in moving one material through another.

Additionally, since Lee and Applicant's Prior Art are both from the same field of endeavor, the purpose disclosed by Applicant's Prior Art would have been recognized in the pertinent art of Lee.

b) increased width portion.

However, Malik discloses a groove formed with an increased width portion (For Example: See Figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a groove with an increased width portion as disclosed in Malik because it aids in isolating various integrated semiconductor devices.

Additionally, since Lee and Malik are both from the same field of endeavor, the purpose disclosed by Malik would have been recognized in the pertinent art of Lee.

7. Claims 6-8 are rejected under 35 U.S.C. 103(a) as obvious over Lee (U.S. Patent No. 5,959,322) in view of Malik et al. (U.S. Patent No. 6,294,423), Applicant's Prior Art and Hieda et al. (U.S. Patent No. 5,508,541).

In regards to claim 6, Lee discloses the following:

a) a word line connected to the gate electrode (34) of said transistor and a bit line (44) coupled to the second diffusion layer of said transistor said word line and said bit line being continuously disposed to cross each other (For Example: See Figure 2).

In regards to claim 6, Lee fails to disclose the following:

a) semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film formed and buried deep enough to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region.

However, Hieda et al. ("Hieda") discloses a semiconductor layer divided into multiple regions (For Example: See Figure 1). It would have been obvious to one having ordinary skill in

the art at the time the invention was made to modify the semiconductor device of Lee to include a semiconductor layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

Additionally, since Lee and Hieda are both from the same field of endeavor, the purpose disclosed by Hieda would have been recognized in the pertinent art of Lee.

In regards to claim 7, Lee discloses the following:

a) bit line is in contact with said second diffusion layer of each DRAM cell at a position adjacent to word lines (For Example: See Figure 2).

In regards to claim 7, Lee fails to disclose the following:

a) element regions.

However, Hieda discloses a semiconductor layer divided into multiple regions (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a semiconductor layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

b) a body wire lead is formed to be contacted with said semiconductor layer across central part of said element region for applying a fixed potential to said semiconductor layer.

However, Hieda discloses a polysilicon layer (60) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a polysilicon layer as disclosed in Hieda because it aids in providing a connection among the various components.

Additionally, since Lee and Hieda are both from the same field of endeavor, the purpose disclosed by Hieda would have been recognized in the pertinent art of Lee.

In regards to claim 8, Lee discloses the following:

a) a word line connected to the gate electrode of said transistor and a bit line coupled to the second diffusion layer of said transistor said word line and said bit line being continuously disposed across each other (For Example: See Figure 2).

In regards to claim 8, Lee fails to disclose the following:

a) semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film formed and buried with a depth failing to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region.

However, Hieda discloses a semiconductor layer divided into multiple regions (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a semiconductor layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

Additionally, since Lee and Hieda are both from the same field of endeavor, the purpose disclosed by Hieda would have been recognized in the pertinent art of Lee.

8. Claim 21 is rejected under 35 U.S.C. 103(a) as obvious over Lee (U.S. Patent No. 5,959,322) in view of Malik et al. (U.S. Patent No. 6,294,423) and Applicant's Prior Art.

In regards to claim 21, Lee discloses the following:

a) an element substrate including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed there between (For Example: See Figure 2);

b) element substrate having a groove formed therein (For Example: See Figures 2, 8 and 14);

c) a trench capacitor (16) formed under said dielectric film to have a storage electrode as half buried in said groove (For Example: See Figure 7);

d) an impurity diffusion source buried in said groove to serve as a buried strap, bottom surface and top surface of said impurity diffusion source being contacted with said storage electrode and bottom surface of said semiconductor layer (For Example: See Figure 2 and Abstract); and

d) a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode , said transistor constituting a DRAM cell with said trench capacitor (For Example: See Figure 2 and 14).

In regards to claim 21, Lee fails to disclose the following:

a) groove formed therein with a depth extending from a top surface of said semiconductor layer into the inside of said semiconductor substrate after penetration through said dielectric film.

However, Malik discloses a groove extending from a top surface of said semiconductor layer into the inside of said semiconductor substrate (16) after penetration through said dielectric film (22 and 20) (For Example: See Figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a groove extending from a top surface of said semiconductor layer into the inside of said semiconductor substrate after penetration through said dielectric film a groove with an increased width portion as disclosed in Malik because it aids in isolating various integrated semiconductor devices.

b) groove being formed to have an increased width portion in said dielectric film, said dielectric film of said increased width portion being receded laterally as to expose a bottom surface of said semiconductor layer and such that the width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer.

However, Malik discloses a groove formed with an increased width portion that exposes the bottom and the width of the groove in the dielectric film is greater than that of the groove in

the semiconductor layer (For Example: See Figure 5, Figure 10 and Column 1 Lines 34-48). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a groove with an increased width portion and the width of the groove in the dielectric film is greater than that of the groove in the semiconductor layer as disclosed in Malik because it aids in isolating various integrated semiconductor devices.

Additionally, since Lee and Malik are both from the same field of endeavor, the purpose disclosed by Malik would have been recognized in the pertinent art of Lee.

c) a cap insulation film formed in said groove.

However, Applicant's Prior Art discloses cap insulation film (4) (For Example: See Figure 37). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include cap film as disclosed in Applicant's Prior Art because it aids keeping the device from shortening out.

Additionally, since Lee and Applicant's Prior Art are both from the same field of endeavor, the purpose disclosed by Applicant's Prior Art would have been recognized in the pertinent art of Lee.

9. Claims 24-26 are rejected under 35 U.S.C. 103(a) as obvious over Lee (U.S. Patent No. 5,959,322) in view of Malik et al. (U.S. Patent No. 6,294,423), Applicant's Prior Art and Hieda et al. (U.S. Patent No. 5,508,541).

In regards to claim 24, Lee discloses the following:

a) a word line connected to the gate electrode of said transistor and a bit line coupled to the second diffusion layer of said transistor said word line and said bit line being continuously disposed to cross each other (For Example: See Figure 2).

In regards to claim 24, Lee fails to disclose the following:

a) semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film formed and buried deep enough to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region.

However, Hieda discloses a semiconductor layer divided into multiple regions (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a semiconductor layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

Additionally, since Lee and Hieda are both from the same field of endeavor, the purpose disclosed by Hieda would have been recognized in the pertinent art of Lee.

In regards to claim 25, Lee discloses the following:

a) bit line is in contact with said second diffusion layer of each DRAM cell at a position adjacent to word lines (For Example: See Figure 2).

In regards to claim 25, Lee fails to disclose the following:

a) element regions.

However, Hieda discloses a semiconductor layer divided into multiple regions (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a semiconductor layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

b) a body wire lead is formed to be contacted with said semiconductor layer across central part of said element region for applying a fixed potential to said semiconductor layer.

However, Hieda discloses a polysilicon layer (60) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a polysilicon layer as disclosed in Hieda because it aids in providing a connection among the various components.

Additionally, since Lee and Hieda are both from the same field of endeavor, the purpose disclosed by Hieda would have been recognized in the pertinent art of Lee.

In regards to claim 26, Lee discloses the following:

a) a word line connected to the gate electrode of said transistor and a bit line coupled to the second diffusion layer of said transistor said word line and said bit line being continuously disposed across each other (For Example: See Figure 2).

In regards to claim 26, Lee fails to disclose the following:

a) semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film formed and buried with a depth failing to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region.

However, Hieda discloses a semiconductor layer divided into multiple regions (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Lee to include a semiconductor layer divided into multiple layers as disclosed in Hieda because it aids in improving high integration density.

Additionally, since Lee and Hieda are both from the same field of endeavor, the purpose disclosed by Hieda would have been recognized in the pertinent art of Lee.

Allowable Subject Matter

10. Claims 4, 5, 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments filed 4/28/03 have been fully considered but they are not persuasive. Applicant argues that "there is no disclosure in Malik that the trench is formed to have an increased width portion such that the bottom of the semiconductor layer is exposed and such that the width of the increased width portion is greater than that of the groove in the semiconductor layer." However, Malik does disclose the limitations listed above (For Example: See Figure 5, Figure 10, Column 1 Lines 5-67 and Column 2 Lines 1-39).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

July 2, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800